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Assembled Individual Disclosure / Adjustment Architecture For Action Appreciation Enumerating Arrays

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Abstract – this paper we propose the objective of DFT is to increase the ease with which a device can be tested to guarantee high system reliability. Among these techniques, BIST has an obvious advantage in that expensive test equipment is not needed and tests are low cost. Moreover, BIST can generate test simulations and analyze test responses without outside support, making tests and diagnoses of digital systems quick and effective. However, as the circuit complexity and density increases, the BIST approach must detect the presence of faults and specify their locations for subsequent repair. The extended techniques of BIST are assembled-in individual-diagnosis and assembled-in individual-re-pair (BISR).This work develops an assembled-in individual-disclosure/adjustment (BISDC) architecture for action appreciation enumerateing arrays (MECAs). Based on the error disclosure/adjustment concepts of biresidue codes, any single error in each processing element in an MECA can be effectively detected and corrected online using the proposed BISD and assembled-in individual-adjustment circuits. Performance analysis and evaluation demonstrate that the proposed BISDC architecture performs well in error disclosure and adjustment with minor area overhead.

Keywords: Digital Video Compression, Optical Flow, Detector, transmission bandwidth, macro Blocks.

I.INTRODUCTION

As the multimedia and wireless technologies become mature, more and more sophisticated portable multimedia applications, such as video cellular phone and hand-held digital video camcorders, are becoming available. Real-time video compression is required to reduce the bandwidth, either for transmission or for storage of video data. However, it consumes a lot of power.

Integrating the MECA into a system-on-chip (SOC) design has become increasingly important for video coding applications.

Although advances in VLSI technology [1] allow integration of a large number of processing elements (PEs) in an MECA into an SOC, this increases the logic-per-pin ratio, thereby significantly decreasing the efficiency of chip logic testing. For a commercial chip, a video coding system must introduce design for testability (DFT), especially in an MECA.

The objective of DFT is to increase the ease with which a device can be tested to guarantee high system reliability. Many DFT approaches have been developed. These approaches can be divided into three categories: ad hoc (problem oriented), structured, and assembled-in individual-test (BIST)[5]. Among these techniques, BIST has an obvious advantage in that expensive test equipment is not needed and tests are low cost.Generally, action appreciation enumerateing array (MECA) performs up to 50% of computations in the entire video coding system (VCS).In VCS, Video data needs to be compressed before storage and transmission, complex algorithms are required to eliminate the redundancy, extracting the redundant information.Action Appreciation (ME) is the process of creating action vectors to track the action of objects within video footage. It is an essential part of many compression standards and is a crucial component of the H.264 video compression standard .In particular; ME can consist of over 40% of the total computation.

Action appreciation is the technique of finding a suitable Action Vector (MV) that best describes the movement of a set of pixels from its original position within one frame to its new positions in the subsequent frame. Encoding just the action vector for the set of pixels requires significantly less bits than what is required to encode the entire set of pixels, while still retaining enough information to reproduce the original video sequence.

A standard movie, which is also known as action picture, can be defined as a sequence of several scenes. A scene is then defined as a sequence of several seconds of action recorded without interruption. A scene usually has at least three seconds. A movie in the cinema is shown as a sequence of still pictures, at a rate of 24 frames per second. Similarly, a TV broadcast consists of a transmission of 30 frames per second (NTSC, and some flavors of PAL, such as PAL-M), 25 frames per second (PAL, SECAM) or anything from 5 to 30 frames per second for typical videos in the Internet.

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The name action picture comes from the fact that a video, once encoded, is nothing but a sequence of still pictures that are shown at a reasonably high frequency. That gives the viewer the illusion that it is in fact a continuous animation. Each frame is shown for one small fraction of a second, more precisely 1/ *k* seconds, where *k* is the number of frames per second. Coming back to the definition of a scene, where the frames are captured without interruption, one can expect consecutive frames to be quite similar to one another, as very little time is allowed until the next frame is to be captured. With all this in mind we can finally conclude that each scene is composed of at least $3 \times k$ frames (since a scene is at least 3 seconds long). In the NTSC case, for example, that means that a movie is composed of a sequence of various segments (scenes) each of which has at least 90 frames similar to one another.

II.SYSTEM OVERVIEW

I. ACTION APPRECIATION

Action appreciation is the process of determining action vectors that describe the transformation from one 2D image to another; usually from adjacent frames in a video sequence. It is an ill-posed problem as the action is in three dimensions but the images are a projection of the 3D scene onto a 2D plane. The action vectors may relate to the whole image (global action appreciation) or specific parts, such as rectangular blocks, arbitrary shaped patches or even per pixel. The action vectors may be represented by a translational model or many other models that can approximate the action of a real video camera, such as rotation and translation in all three dimensions and zoom.

Closely related to action appreciation is optical flow, where the vectors correspond to the perceived movement of pixels. In action appreciation an exact 1:1 correspondence of pixel positions is not a requirement. Applying the action vectors to an image to synthesize the transformation to the next image is called action compensation. The combination of action appreciation and action compensation is a key part of video compression as used by MPEG 1, 2 and 4 as well as many other video codecs.

A. Algorithms:

B. The methods for finding action vectors can be categorized into pixel based methods ("direct") and feature based methods ("indirect"). A famous debate resulted in two papers from the opposing factions being produced to try to establish a conclusion.

1) Direct Methods:

- Block-matching algorithm
- Phase correlation and frequency domain methods
- Pixel recursive algorithms
- MAP/MRF type "Bayesian" estimators
- Optical flow

a) Evaluation Metrics:

In direct methods several evaluation metrics can be used.

- Mean squared error (MSE)
- Sum of absolute differences (SAD)
- Mean absolute difference (MAD)
- Sum of squared errors (SSE)
- Sum of absolute transformed differences (SATD)

2) Indirect Methods:

Indirect methods use features, such as Harris corners, and match corresponding features between frames, usually with a statistical function applied over a local or global area. The purpose of the statistical function is to remove matches that do not correspond to the actual action. Statistical functions that have been successfully used include RANSAC.

Digital Video Compression

Video compression is achieved on two separate fronts by eliminating spatial redundancies and temporal redundancies from video signals. Removing spatial redundancies involves the task of removing video information that is consistently repeated within certain areas of a single frame. For example a frame shot of a blue sky will have a consistent shade of blue across the entire frame. This information can be compressed through the use of various discreet cosine transformations that map a given image in terms of its light or color intensities. This paves the way for spatial compression by only capturing the distinct intensities, instead of the spread of intensities over the entire frame. Since compression through removing spatial redundancies does not involve the use of action appreciation, this topic is not examined further.

Compression through the removal of temporal redundancies involves compressing information that is repeated over a given sequence of frames. For example the objects in the background of a news anchor being filmed are not likely to change over the course of the footage. This redundancy can be taken advantage of to reduce the storage space required for the footage. When the background does happen to move, recording only the action of objects over consecutive frames in the form of action vectors can still achieve significant amounts of compression. Consequently, the action appreciation process is the process of deriving a suitable Action Vector (MV) that best describes the spatial movement of objects from one frame to the next.

By using this temporal redundancy and spatial redundancy we can reduce the storage space and transmission bandwidth. The spatial and temporal compression techniques discussed above have been widely implemented in former compression standards such as MPEG 2 (developed by the Action Picture Experts Group committee). At present, the same two fundamental techniques have been enhanced and optimized to form the new standard used in H.264 video compression.

The H.264 standard was jointly formed by the International Telecommunications Union – Telecommunications Standardization Sector (ITU – T) Video Coding Experts

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Group (VCEG) and the International Organization for Standardization (ISO) MPEG committee. MPEG 2 had compression ratios of between 20:1 and 30:1, the new H.264 standard can achieve compression ratios as high as 50:1 and 60:1 and achieve better video quality. Among many other new features and enhancements, the most notable features of the H.264 standard for this work are its ability to achieve a finer granularity of action appreciation and its ability to capture periodic action.

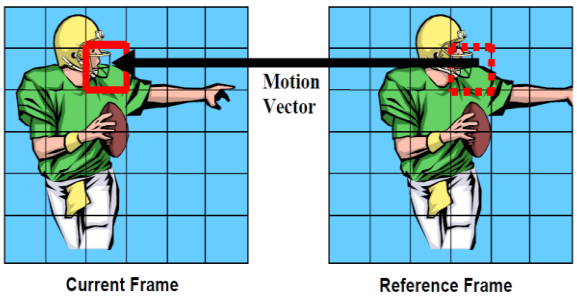
Block Matching Action Appreciation

Several different algorithms derived from various theories, including object-oriented tracking, exist to perform action appreciation. Among them, one of the most popular algorithms is the Block Matching Action Appreciation (BME) algorithm. BME treats a frame as being composed of many individual sub-frame blocks, known as macro Blocks. Action vectors are then used to encode the action of the macro Blocks through frames of video via a frame by frame matching process.

When a frame is brought into the encoder for compression, it is referred to as the current frame. It is the goal of the BME unit to describe the action of the macro Blocks within the current frame relative to a set of reference frames. The reference frames may be previous or future frames relative to the current frame. Each reference frame is also divided into a set of sub-frame blocks, which are equal to the size of the macro Blocks. These blocks are referred to as reference Blocks.

The BME algorithm will scan several candidate reference Blocks within a reference frame to find the best match to a macro Block. Once the best reference Block is found a action vector is then calculated to record the spatial displacement of the macro Block relative to the matching reference Block, as shown in Figure.

Fig : Block Matching between Current & reference frames



III.THE WORKING PRINCIPLE

In information theory and coding theory with applications in computer science and telecommunication, error disclosure and adjustment or error control are techniques that enable reliable delivery of digital data over unreliable communication channels. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error disclosure techniques allow detecting such errors, while error adjustment enables reconstruction of the original data. The general idea for achieving error disclosure and adjustment is to add some redundancy (i.e., some extra data) to a message, which receivers can use to check consistency of the delivered message, and to recover data determined to be erroneous. Error-disclosure and adjustment schemes can be either systematic or non-systematic: In a systematic scheme, the transmitter sends the original data, and attaches a fixed number of *check bits* (or *parity data*), which are derived from the data bits by some deterministic algorithm. If only error disclosure is required, a receiver can simply apply the same algorithm to the received data bits and compare its output with the received check bits; if the values do not match, an error has occurred at some point during the transmission. In a system that uses a non-systematic code, the original message is transformed into an encoded message that has at least as many bits as the original message. Good error control performance requires the scheme to be selected based on the characteristics of the communication channel. Common channel models include memory-less models where errors occur randomly and with a certain probability, and dynamic models where errors occur primarily in bursts. Consequently, error-detecting and correcting codes can be generally distinguished between *random-error-detecting/correcting* and burst-error-detecting/correcting. Some codes can also be suitable for a mixture of random errors and burst errors. If the channel capacity cannot be determined, or is highly varying, an error-disclosure scheme may be combined with a system for retransmissions of erroneous data. This is known as automatic repeat request (ARQ), and is most notably used in the Internet. An alternate approach for error control is hybrid automatic repeat request (HARQ), which is a combination of ARQ and error-adjustment coding.

C. Implementation

Error adjustment may generally be realized in two different ways:

Automatic repeat request (ARQ) (sometimes also referred to as backward error adjustment): This is an error control technique whereby an error disclosure scheme is combined with requests for retransmission of erroneous data. Every block of data received is checked using the error disclosure code used, and if the check fails, retransmission of the data is requested – this may be done repeatedly, until the data can be verified. Forward error adjustment (FEC): The sender encodes the data using an error-correcting code (ECC) prior to transmission. The additional information (redundancy) added by the code is used by the receiver to recover the original data. In general, the reconstructed data is what is deemed the "most likely" original data. ARQ and FEC may

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be combined, such that minor errors are corrected without retransmission, and major errors are corrected via a request for retransmission: this is called hybrid automatic repeat-request (HARQ).

IV.IMPLEMENTATION OF SYSTEM

DETECTOR:

Detector module will detect whether there is an error in output of PE i.e. SAD. Here the Error is calculated. The output of PE and theoretically calculated SAD will be subtracted which is given as e = SAD'-SAD.

SELECTOR:

Selector takes the output of the processing element as an input. Another input to the selector is the output of the detector. If the Detector block detects any error in the PE output then the Selector block will give the PE output to Syndrome Decoder to detect in which bit position there is an error and also to the Corrector block to correct the single bit error.

SYNDROME DECODER:

This module decodes the syndrome values which specify the error bit position in the SAD. Syndromes can be expressed as

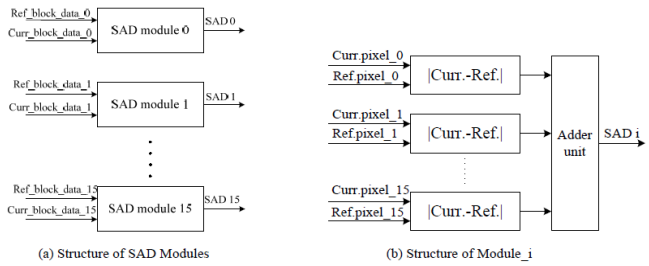
$(S\varphi_1, S\varphi_2) = (|N'_j - X|_{\varphi 1}, |N'_j - Y|_{\varphi 2}) = (|e|_{\varphi 1}, |e|_{\varphi 2})$

CORRECTOR:

Input to the corrector module is the output of the selector module which is SAD that needs to be corrected; the bit position which needs adjustment is specified by the syndrome decoder. The corrector architecture consists of LUT and 12 multiplexers.

PE ARRAY ARCHITECTURE

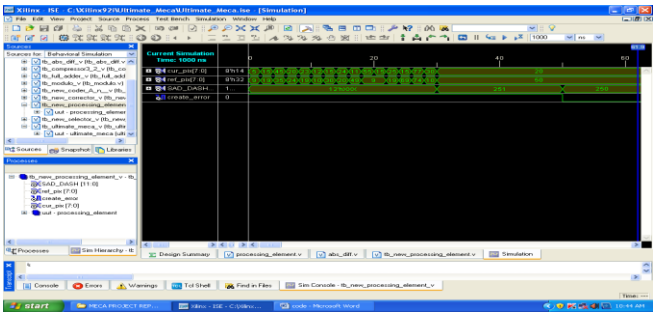
PE is a module that calculates the absolute difference between the pixel of the reference block and the pixel of the current block. Fig. 4.1 shows the architecture of PE Array 4x4.To enable the reference data shifting to top, bottom, right or left in PE Array 4x4, each PE is connected to the PE of top, bottom, right or left one. This structure generates SAD 4x1 by accumulating the absolute difference of each PE. Furthermore, SAD 4x4 is generated by accumulating generated SAD 4x1.



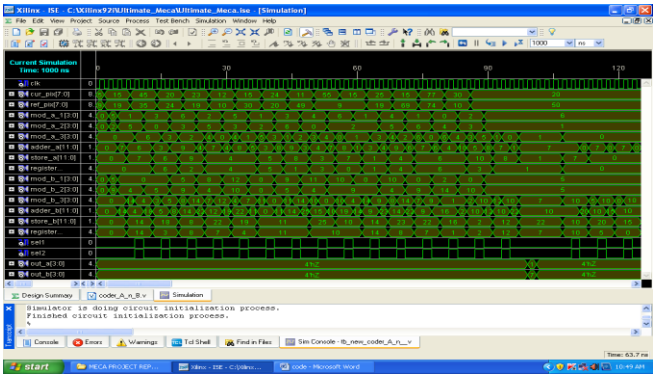
Basic structure of SAD Modules

V.EXPERIMENTAL RESULTS

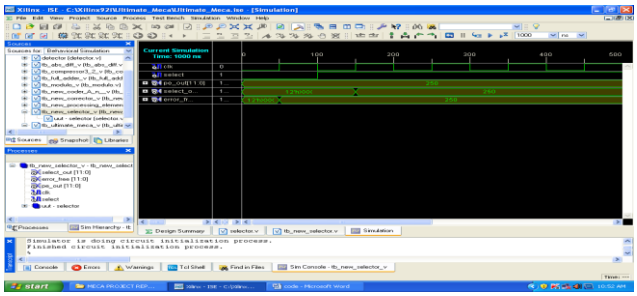
Top Module Simulation waveforms



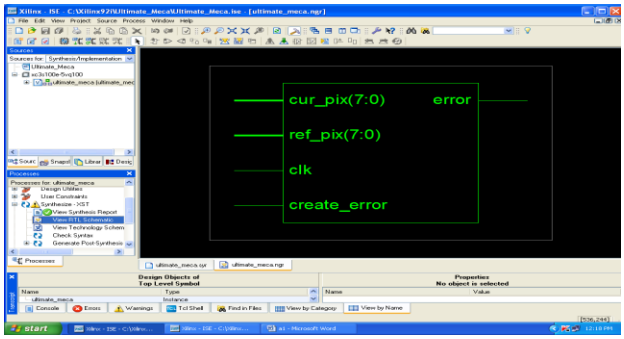
Processing Element module



Coder module



SELECTOR module



RTL SCHEMATIC RESULT:

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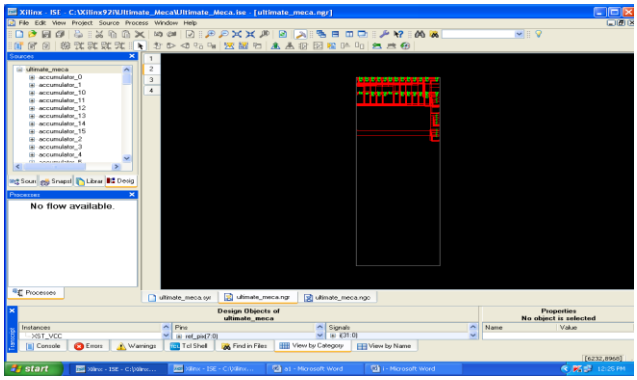

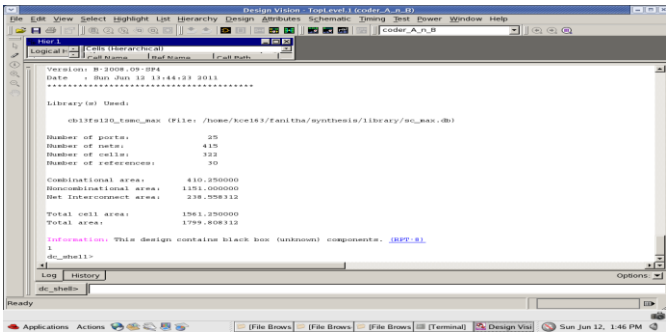

area of coder module using 120nm technology

VI.CONCLUSION

Moreover, BIST can generate test simulations and analyze test responses without outside support, making tests and diagnoses of digital systems quick and effective. However, as the circuit complexity and density increases, the BIST approach must detect the presence of faults and specify their locations for subsequent repair. The extended techniques of BIST are assembled-in individual-diagnosis and assembled-in individual-re- pair (BISR).This work develops a assembled-in individual-disclosure/adjustment (BISDC) architecture for action appreciation enumerateing arrays (MECAs). Based on the error disclosure/adjustment concepts of biresidue codes[2], any single error in each processing element in an MECA can be effectively detected and corrected online using the proposed BISD and assembled-in individual-adjustment circuits. The input to the MECA is taken in binary format. By Adding the Image to Bit Converter input to MECA is directly in the form of frames, timing required for Action Appreciation will be reduced. The input to the MECA is 8-bit data. It also can be extended to higher volume of data. But the Calculation time required is also high.

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